NANO SCIENTIFIC RESEARCH CENTRE
An ISO: 9001:2008 Certified Company
#604, Siri Estates, Opp. Lane to R.S. Brothers, Ameerpet, Hyderabad-500073.
E-mail: info@nanocdac.com, www.nanocdac.com +91-8297578555, +91-9640648777

MTECH IEEE VLSL PROJECTS

S.NO	CODE	TITLE
1	SDVL 01	Area-Efficient Intellectual Property (IP) Design of Advanced EncryptionStandard
2	SDVL 02	On the Design of Iterative Approximate Floating-Point Multipliers
3	SDVL 03	AxPPA: Approximate Parallel Prefix Adders
4	SDVL 04	Designs of BCD Adder Based on Excess-3 Code in Quantum-Dot CellularAutomata
5	SDVL 05	Multiple-Mode-Supporting Floating-Point FMA Unit for Deep LearningProcessors
6	SDVL 06	A Stochastic Computing Sigma-Delta Adder Architecture for EfficientNeural Network Design
7	SDVL 07	DACA: Dynamic Accuracy-Configurable Adders for Energy-EfficientMulti-Precision Computing
8	SDVL 08	A Low Latency Approximate Adder Design based on Dual Sub-Adderswith Error Recovery
9	SDVL 09	Parallel Prefix Modulo-$(2^q + 2^{q-1} + 1)$ Adder via Diminished-1Representation of Residues
10	SDVL 10	Design of Optimal Multiplier less FIR Filters With Minimal Number ofAdders
11	SDVL 11	Synthesis of Approximate Parallel-Prefix Adders
12	SDVL 12	LSAC: A Low-Power Adder Tree for Digital Computing-in-Memory bySparsity and Approximate Circuits Co-Design
13	SDVL 13	IMPLY-Based High-Speed Conditional Carry and Carry Select Adders forIn-Memory Computing
14	SDVL 14	Efficient Digital Implementation of a Multirate-Based Variable FractionalDelay Filter for Wideband Beam forming
15	SDVL 15	Hardware Efficient 2-Parallel and 3-Parallel Even Length FIR FiltersUsing FFA
16	SDVL 16	Low Area and Low Power Threshold Implementation Design Techniquefor AES S-Box
17	SDVL 17	Simplified Compressor and Encoder Designs for Low-Cost ApproximateRadix-4 Booth Multiplier

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18	SDVL 18	AsteRISC: A Size-Optimized RISC-V Core for Design Space Exploration
19	SDVL 19	Area Efficient Approximate 4-2 Compressor and Probability-Based ErrorAdjustment for Approximate Multiplier
20	SDVL 20	Efficient Approximate Multiplier Design Based on Hybrid Higher RadixBooth Encoding
21	SDVL 21	Exact Versus Inexact Decimal Floating-Point Numbers and Arithmetic
22	SDVL 22	Low-Power Reconfigurable FIR Filter Design Based on CommonOperation Sharing
23	SDVL 23	Hybrid Protection of Digital FIR Filters
24	SDVL 24	Multi-Sinusoidal Perturbation Strategy for BPSK Power Line Communication and Online Battery Impedance Measurement
25	SDVL 25	Approximate Softmax Functions for Energy-Efficient Deep NeuralNetworks
26	SDVL 26	A High-Throughput and Flexible Architecture Based on a Reconfigurable Mixed-Radix FFT With Twiddle Factor Compression and Conflict-FreeAccess
27	SDVL27	A High-Speed FPGA-Based True Random Number Generator UsingMetastability With Clock Managers
28	SDVL 28	High-Throughput Low-Latency Pipelined Divider for Single-Precision Floating-Point Numbers
29	SDVL 29	BCD Adder Designs Based on Three-Input XOR and Majority Gates
30	SDVL 30	Area-Efficient Nano-AES Implementation for Internet-of-Things Devices