NANO SCIENTIFIC RESEARCH CENTRE

(An ISO: 9001:2008 Certified Company)

#604, Opp. Lane to R.S. Brothers, Siri Estates, Ameerpet, Hyderabad, Telangana 500073.
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VLSI: B.Tech IEEE Project List

CODE	TITLES
NVD-01	Dual-Quality 4:2 Compressors for Utilizing in Dynamic Accuracy Configurable Multipliers
NVD-02	Design of Power and Area Efficient Approximate Multipliers
NVD-03	Low power Viterbi decoder design based on reversible logic gates
NVD-04	Modified carry select adder for power and area reduction
NVD-05	Low Power Array Multiplier Using Modified Full Adder
NVD-06	Design of Efficient BCD Adders in Quantum-Dot Cellular Automata
NVD-07	Reconfigurable delay optimized carry select adder
NVD-08	Low Power Array Multiplier Using Modified Full Adder
NVD-09	A Modified Partial Product Generator for Redundant Binary Multipliers
NVD-10	Reconfigurable Constant Multiplication for FPGAs
NVD-11	On the VLSI Energy Complexity of LDPC Decoder Circuits
NVD-12	VLSI Design for Convolutive Blind Source Separation
NVD-13	10T SRAM Using Half-VDD Precharge and Row-Wise Dynamically Powered Read Port for Low Switching Power and Ultralow RBL Leakage
NVD-14	A Cellular Network Architecture With Polynomial Weight Functions
NVD-15	IMPLEMENTATION OF REDUNDANT BINARY HIGH SPEED MULTIPLIERS WITHEFFICIENT PARTIAL PRODUCT GENERATOR
NVD-16	A Normal I/O Order Radix-2 FFT Architecture to Process TWIN DATA STREAMS FOR MIMO
NVD-17	Iterative Architecture AES for Secure VLSI basedSystem Design
NVD-18	VLSI Implementation of 3D Integer DCT for Video Coding Standards
NVD-19	Optimized implementation of FFT processor for OFDM systems
NVD-20	Power delay product optimized hybrid full added circuits

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NVD-21	RoBA Multiplier: A Rounding-Based Approximate Multiplier for High-Speed yet Energy-Efficient Digital Signal Processing
NVD-22	Multifunction Residue Architectures for Cryptography
NVD-23	Fault Tolerant Parallel FFTs Using Error Correction Codes and Parseval Checks
NVD-24	Low-Complexity Tree Architecture for Finding the First Two Minima
NVD-25	LOW POWER AREA EFFICIENT ALU WITH LOW POWER FULL ADDER
NVD-26	Aging-Aware Reliable Multiplier Design With Adaptive Hold Logic
NVD-27	Reconfigurable Constant Multiplication for FPGAs
NVD-28	Low-Power and Area-Efficient Shift Register UsingPulsed Latches
NVD-29	Analysis of vedic multiplier using various adder topologies.
NVD-30	An Efficient Constant Multiplier Architecture Based on Vertical-Horizontal Binary Common Sub-expression Elimination Algorithm for Reconfigurable FIR Filter Synthesis
NVD-31	Fault Tolerant Parallel FFTs Using Error Correction Codes and Parseval Checks
NVD-32	Scan Test Bandwidth Management for Ultralarge-Scale System-on-Chip Architectures

VLSI: B.Tech/M.E IEEE Project List

NV1601	Floating-Point Butterfly Architecture Based on Binary Signed-Digit Representation
NV1602	Flexible DSP Accelerator Architecture Exploiting Carry-Save Arithmetic
NV1603	Utilizing Shared Memory Multi-cores to Speed-up the ATPG process
NV1604	Fault Tolerant Parallel Filters Based on Error Correction Codes
NV1605	Error Correction Technique Based on Modular Correcting Codes
NV1606	FPGA Based Rate Compatible LDPC Codes for The Next Generation of Optical Transmission Systems
NV1607	A Modified Partial Product Generator for Redundant Binary Multipliers
NV1608	A High-Throughput Energy-Efficient Implementation of Successive Cancellation Decoder for Polar Codes Using Combinational Logic
NV1609	On Optimization-based ATPG and its Application for Highly Compacted Test Sets
NV1610	High-Performance Pipelined Architecture of Elliptic Curve Scalar Multiplication Over GF(2^m)m
NV1611	Fault Tolerant Parallel FFTs Using Error Correction Codes and Parseval Checks
NV1612	A High-Throughput Energy-Efficient Implementation of Successive Cancellation Decoder for Polar Codes Using Combinational Logic
NV1613	Low-Power Parallel Chien Search Architecture Using a Two-Step Approach

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NV1614	Memory-Reduced Turbo Decoding Architecture Using NII Metric Compression Logic
NV1615	A Normal I/O Order Radix-2 FFT Architecture to Process Twin Data Streams for MIMO
NV1616	A High-Performance FIR Filter Architecture for Fixed and Reconfigurable Applications

CODE	B,TECH VLSI IEEE PROJECTS
NV1501	ADynamicallyReconfigurableMulti-ASIPArchitectureforMultistandard and Multimode Turbo Decoding
NV1502	Low-Cost High-PerformanceVLSIArchitectureforMontgomeryModular Multiplication
NV1503	Functional Constraint Extraction From RegisterTransferLevel for ATPG
NV1504	Fault Tolerant Parallel Filters Based on Error Correction Codes
NV1505	DScanPUF: A Delay-Based Physical Unclonable Function Built Into Scan Chain
NV1506	Pre-Encoded Multipliers Based on Non-Redundant Radix-4 Signed-Digit Encoding
NV1507	Quantumcostrealizationofnewreversiblegateswithtransformationbased synthesis technique
NV1508	On the Analysis of Reversible Booth's Multiplier
NV1509	Optimized Logarithmic Barrel Shifter in Reversible Logic Synthesis
NV1510	A novel delay& Quantum Cost efficientreversiblerealizationof2i× j Random Access Memory
NV1511	Exploiting Same Tag Bits to Improve the Reliability of the Cache Memories
NV1512	Hardware Efficient MixedRadix-25/16/9FFT for LTE Systems
NV1513	Energy-Efficient Approximate Multiplication for Digital Signal Processing and Classification Applications
NV1514	A Combined SDC-SDF Architecture for Normal I/O Pipelined Radix-2 FFT
NV1515	An Accuracy-Adjustment Fixed-Width Booth Multiplier Based on Multilevel Conditional Probability
NV1516	Design and ASIC Implementation of Column Compression Wallace/Dadda Multiplier in Sub-Threshold Regime
NV1517	Novel Design Algorithm for Low Complexity Programmable FIR Filters Based on Extended Double Base Number System
NV1518	An Efficient VLSI Architecture of a Reconfigurable Pulse-Shaping FIR Interpolation Filter for Multistandard DUC
NV1519	(4 + 2 log n)ΔG Parallel Prefix Modulo-(2n − 3)Adder via Double Representation of Residues in [0, 2]
NV1520	Low-Complexity Tree Architecture for Finding the First Two Minima
NV1521	A Generalized Algorithm and Reconfigurable Architecture for Efficient and Scalable Orthogonal Approximation of DCT
NV1522	High-Throughput Finite Field Multipliers Using Redundant Basis for FPGA and ASIC Implementations
NV1523	Test Data Compression using Hamming Encoder and Decoder for System On Chip (SOC) Testing
NV1524	Self-Repairing Digital System With Unified Recovery Process Inspired by Endocrine Cellular Communication
NV1525	Fully Reused VLSI Architecture of FM0/Manchester Encoding Using SOLS Technique for DSRC Applications
NV1526	Partially Parallel Encoder Architecture for Long Polar Codes
NV1527	Z-TCAM: An SRAM-based Architecture for TCAM
NV1528	Digital Post-Correction of Analog-to-Digital Converters with Real-Time FPGA Implementation
NV1429	Low-Complexity Low-Latency Architecture for Matching of Data Encoded With Hard Systematic Error-Correcting Codes

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NV1430	Energy-Efficient High-Throughput Montgomery Modular Multipliers for RSA Cryptosystems
NV1431	A Class of SEC-DED-DAE C Codes Derived From Orthogonal Latin Square Codes
NV1432	Efficient FPGA and ASIC Realizations of a DA-Based Reconfigurable FIR Digital filter
NV1433	Low-Power Digital Signal Processor architecture For WirelessSensorNodes
NV1334	Error Detection in Majority Logic Decoding of Euclidean GeometryLow Density Parity Check(EG-LDPC)Codes
NV1335	Low-Power, High-Throughput, and Low-Area Adaptive FIR Filter Based On Distributed Arithmetic
NV1336	Radix-4andradix-8booth encoded multi-modulus multipliers
NV1337	Design and Implementation of an On-Chip Permutation Network for Multiprocessor System-On-Chip
NV1338	Multi operand Redundant Adders on FPGA's
NV1339	Globalbuilt-inself-repairfor3Dmemorieswithredundancysharing and Parallel testing
NV1340	A Practical NoC Design for Parallel DES Computation
NV1341	Parallel AES Encryption Engines for Many-Core Processor Arrays
NV1342	VLSI Implementation of a HighSpeedSinglePrecisionFloatingPointUnit Using Verilog
NV1343	A VLIW Architecture for Executing Multi-Scalar/Vector Instructions on Unified Data path
NV1344	A Novel Modulo Adder for 2n-2k-1Residue Number System
NV1345	Low-cost FIR filter designs based on faithfully rounded truncated Multiple constant multiplication/accumulation
NV1346	Low-Power, High-Throughput, and Low-Area Adaptive FIR Filter Based On Distributed Arithmetic
NV1347	Design and Implementation of 32 Bit Unsigned Multiplier Using CLAA and CSLA
NV1348	Enhanced Area Efficient Architecture for128 bit Modified CSLA
NV1349	High Performance Hardware Implementation of AES Using Minimal Resources
NV1350	Implementation of I2C Master Bus Controller on FPGA
NV1351	Novel High Speed Vedic Mathematics Multiplier using Compressors
NV1352	VLSI Implementation of a HighSpeedSinglePrecisionFloatingPointUnit Using Verilog
NV1353	VLSI implementation of Fast Addition using Quaternary Signed Digit Number System
NV1354	Design of High Performance 64bit MAC Unit
NV1355	FPGA Architecture for OFDM Software Defined Radio with an Optimized Direct Digital Frequency Synthesizer
NV1356	Implementation of UART with BIST Technique in FPGA
NV1357	A High Speed Binary Floating Point Multiplier Using Dadda Algorithm
NV1258	Soft-Error-Resilient FPGAs Using Built-In 2-D Hamming Product Code
NV1259	High-Speed Low-Power Viterbi Decoder Design for TCM Decoders
NV1260	Product Code Schemes for Error Correction in MLC NAND Flash Memories
NV1261	Low-Power and Area-Efficient Carry Select Adder
NV1262	Low-Cost Binary128 Floating-Point FMA Unit Design with SIMD Support
NV1263	Design and Implementation of 64-Bit Execute Stage for VLIW Processor Architecture on FPGA
NV1264	Design and FPGA-based Implementation of a High Performance32-bit DSP Processor

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VLSI BACKEND: LOW POWER VLSI PROJECTS

VLSI: B.Tech/M.E IEEE Project List

CODE	B.Tech VLSI IEEE PROJECTS
NL1601	Optimized Active Single-Miller Capacitor Compensation With Inner Half-Feed forward Stage for Very High-Load Three-Stage OTAs
NL1602	Compensation Method for Multi Stage Opamps with High Capacitive Load Using Negative Capacitance
NL1603	Variable-Mirror Amplifier: A New Family of Process-Independent Class-AB Single-Stage OTAs for Low-Power SC Circuits
NL1604	A Low Noise Output Capacitor-less Low Dropout Regulator with a Switched-RC Band gap Reference
NL1605	Integer-N Phase Locked Loop for Bluetooth Receiver in CMOS 130 nm Technology
NL1606	Ultra-low-power one-pin crystal oscillator with self-charged technique
NL1607	High-Performance Low-Cost Dual 15 GHz/30 GHz CMOS LC Voltage-Controlled Oscillator
NL1608	A Power-Efficient Reconfigurable Output-Capacitor-Less Low-Drop-Out Regulator for Low-Power Analog Sensing Front-End
NL1609	Analysis of 8 Bit RCA Adder at Different Nanometer Regime
NL1610	A Novel Power Efficient N-MOS Based 1-Bit Full Adder
NL1611	Methods of Slew Rate Verification of Operational Amplifier Macro Model
NL1612	A Novel Power Efficient Pulse Triggered Flip Flop with Minimum Transistors
NL1613	Design of Low-Power High-Gain Operational Amplifier for Bio-Medical Applications
NL1614	Low-Complexity Multiternary Digit Multiplier Design in CNTFET Technology
NV1615	A Modified SRAM Based Low Power Memory Design
NV1616	Low Power High Speed D Flip Flop Design using Improved SVL Technique

VLSI: B.Tech/M.E IEEE Project List

CODE	B.Tech VLSI IEEE PROJECTS
NL1501	Low-Power Clock Distribution Using a Current-Pulsed Clocked Flip-Flop
NL1502	Design Methodology of Sub threshold Three-Stage CMOSOT As Suitable for Ultralow-Power Low-Area and High Driving Capability
NL1503	Low–Power and Area-Efficient Shift Register Using Pulsed Latches
NL1504	A Fully-Integrated Low-Dropout Regulator With Full-Spectrum Power Supply Rejection
NL1505	40-Gbs0.7-V21MUXand12DEMUXwithTransformer-Coupled Technique for SerDes Interface
NL1506	Low Power Conditional Pulse Control with Transmission Gate Flip-Flop
NL1507	An Efficient Design Technique for Low Power Dynamic Feed through Logic With Enhanced Performance for wide fan-in gates
NL1508	Performance Analysis of CNTFET Based DigitalLogicCircuits
NL1509	A 90nm Low Power OTA Using Adaptive Bias
NL1510	Implementing Low-Power Dynamic Adders in MTCMOS Technology

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NL1511	Design of high speed ternary full adder and three input XOR circuits using CNTFETs
NL1512	An 8GHz First-Order Frequency Synthesizer for Low-Power On-Chip Clock Generation
NL1513	Free class AB–AB Miller opamp with high current enhancement
NL1514	Ultralow-Energy Variation-Aware Design: Adder Architecture Study
NL1515	Designing Tunable Sub threshold Logic Circuits Using Adaptive Feedback equalization
NL1516	Design of a Low Power 4x4 Multiplier Based on Five Transistor (5-T) Half Adder, Eight Transistor (8-T) Full Adder & Two Transistor (2-T) AND Gate
NL1517	Dynamic Threshold Source Coupled Logic with Push pull topology for Ultra Low Power Applications
NL1518	Low Voltage Full Swing VCO With Symmetrical Even Phase Outputs Based On Single Ended Delay Cells
NL1519	Recursive Approach to the Design of a Parallel Self-Timed Adder
NL1420	Comparative Performance Analysis of XORXNOR Function Based High-Speed CMOS Full Adder Circuits
NL1421	Analysis and Design of a Low-Voltage Low-Power Double-Tail Comparator
NL1422	A Fault-Tolerant Technique using Quadded Logic and Quadded Transistors

***NOTE*: PLEASE CONTACTUS IF ANY ONE IS INTERESTED TO SELECT CADENCE PROJECTS**