VLSI: M.Tech/M.E IEEE Project List 2019-2020

NVD-01	Hardware Design of an Energy-Efficient High-Throughput Median Filter Shih-Hsiang Lin, Pei-Yin Chen, Member, IEEE, and Chang
NVD-02	Area and Power Efficient VLSI Architecture of Distributed Arithmetic Based LMS Adaptive Filter
NVD-03	A High-performance and Area-efficient VLSI Architecture for the PRESENT Lightweight Cipher
NVD-04	Novel High speed Vedic Multiplier proposal incorporating Adder based on Quaternary signed Digit number system
NVD-05	Basic-Set Trellis Min–Max Decoder Architecture for Nonbinary LDPC Codes With High-Order Galois Fields
NVD-06	A Novel Zero Blind Zone Phase Frequency Detector for Fast Acquisition in Phase Locked Loops
NVD-07	Design of Low Power 8-Bit Carry Select Adder Using Adiabatic Logic
NVD-08	Dual-Quality 4:2 Compressors for Utilizing in Dynamic Accuracy Configurable Multipliers
NVD-09	Fm0 and Manchester Encoding Using Sols Technique with Clock Gating & Power Gating Methods
NVD-10	FPGA Implementation of an Improved Watchdog Timer for Safety-critical Applications
NVD-11	A Low-Power Yet High-Speed Configurable Adder for Approximate Computing
NVD-12	A Low-Power High-Speed Accuracy-Controllable Approximate Multiplier Design
NVD-13	Chip Design for Turbo Encoder Module for In-Vehicle System
NVD-14	Efficient Modular Adders based on Reversible Circuits
NVD-15	Power Efficient Approximate Multipliers in LMS Adaptive Filters
NVD-16	MAES: Modified Advanced Encryption Standard for Resource Constraint Environments
NVD-17	Binary To Gray Code Converter Implementation Using QCA
NVD-18	A Low-Power High-Speed Comparator for Precise Applications
NVD-19	A High Performance Gated Voltage Level Translator with Integrated Multiplexer
NVD-20	Low-Power and Fast Full Adder by Exploring New XOR and XNOR Gates
NVD-21	Design of Area-Efficient and Highly Reliable RHBD 10T Memory Cell for Aerospace Applications
NVD-22	High speed and low power preset-able modified TSPC D flip-flop design and performance comparison with TSPC D flip-flop
NVD-23	Low Power 4×4 Bit Multiplier Design using Dadda Algorithm and Optimized Full Adder
NVD-24	Low Leakage Fully Half-Select-Free Robust SRAM Cells with BTI Reliability Analysis
NVD-25	Analysis of vedic multiplier using various adder topologies
NVD-26	Reconfigurable delay optimized carry select adder

NVD-27	Analysis and Design of Low-Power Reversible Carry Select Adder Using D-Latch
NVD-28	Design of Area and Delay Efficient Vedic Multiplier Using Carry Select Adder
NVD-29	An Improved DCM-Based Tunable True Random Number Generator for Xilinx FPGA
NVD-30	Scalable Approach for Power Droop Reduction During Scan-Based Logic BIST
NVD-31	Reconfigurable Constant Multiplication for FPGAs
NVD-32	RoBA Multiplier: A Rounding-Based Approximate Multiplier for High-Speed yet Energy-Efficient Digital Signal Processing
NVD-33	DESIGN OF POWER AND AREA EFFICIENT APPROXIMATE MULTIPLIERS.
NVD-34	DESIGN OF EFFICIENT BCD ADDERS IN QUANTUM-DOT CELLULAR AUTOMATION
NVD-35	Implementation of Multiplier Architecture Using Efficient Carry Select adders for synthesizing FIR filters.
NVD-36	ASIC Implementation of Distributed Arithmetic in Adaptive FIR Filter
NVD-37	VLSI Implementation of Boolean Algebra based Cryptographic Algorithm
NVD-38	Iterative Architecture AES for Secure VLSI based System Design
NVD-39	Novel Structure for Area-Efficient Implementation of FIR Filters
NVD-40	Dual Use of Power Lines for Design-for-Testability—A CMOS Receiver Design
NVD-41	Graph-Based Transistor Network Generation Method for Supergate Design
NVD-42	A Single-Ended With Dynamic Feedback Control 8T Subthreshold SRAM Cell

VLSI: M.TECH/M.E IEEE PROJECT LIST 2017-2018

CODE	M.Tech VLSI IEEE PROJECTS	YEAR
Nvd-01	A normal i/o order radix-2 fft architecture to process twin data streams for mimo	2017
Nvd-02	On optimization-based atpg and its application for highly compacted test sets	2017
Nvd-03	Fault Tolerant parallel filters based on error correction codes	2017
Nvd-04	Fault Tolerant Parallel Ffts Using Error Correction Codes And Parseval Checks	2017
Nvd-05	Low-complexity transformed encoder architectures for quasi-cyclic nonbinary ldpc codes over subfields	2017
Nvd-06	Design and implementation of low power digital fir filter based on low power	2017
Nvd-07	Error correction technique based on modular correcting codes	2017
Nvd-08	An improved design of a reversible fault tolerant lut-based fpga	2017
Nvd-09	Low power hilbert transformer design with reconfigurability using row bypassing multiplier	2017
Nvd-10	Fpga based digital ic tester	2017