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NANO SCIENTIFIC RESEARCH CENTRE

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VERILOG HDL

- Introduction to Verilog HDL
- Modeling Concepts
 - ⊗ Gate Level Modeling
 - ⊗ Data Flow Modeling
 - ⊗ Behavioural Modeling
 - ⊗ Structural Modeling
 - ⊗ Switch Level Modeling
- Data Types
- Operators
- Procedure and Flow Of Control Statement
- Designing of Combinational Circuits
- Designing of Sequential Circuits
- FSM Design Modeling
- Designing of Memories
- Writing Testbench using Verilog
- Task and Functions
- System Tasks
- Compiler Directives
- Advance Nets in Verilog
- Bus Functional Modeling
- Verilog Based Assertions
- Code Coverage.